UCM DUPLINE

Installation and Programming Manual

This Manual describes the UCM applications for interfacing a Carlo Gavazzi Dupline network to a SY/MAX PLC.

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Niobrara Research & Development Corporation
P.O. Box 3418 Joplin, MO 64803 USA

Telephone: (800) 235-6723 or (417) 624-8918
Facsimile: (417) 624-8920
www.niobrara.com

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Introduction

The Niobrara UCM4 is a SY/MAX® compatible module that is capable of running multiple applications for performing communication translations between serial protocols. This document covers a single application that moves I/O data in a SY/MAX PLC to/from a Carlo Gavazzi (Electromatic) Dupline network.

The application is called PORT1.UCM PORT1.UCM is loaded into the UCM's Port 1 and provides the interface to the Optolink Fiber Optic RS-232 interface of the Dupline network. This application was specifically written a specific installation with nine Dupline networks connected by Optolinks.

The UCM4-S version of the UCM is recommended for this application if the fiber optic is close enough for straight RS-232 cabling.

The UCM4-S will be mounted in a SY/MAX register rack and will need to be rack addressed by the PLC for 209 registers to gain access to the I/O for 9 Dupline networks plus statistical information.

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Installation

Module Installation

1 Remove power from the rack.

2 Mount the UCM4-S in an available slot in the register rack. Secure the screw at the bottom of the module.

3 Apply power to the rack.

Software Installation

The application files for the UCM4 are included in the DUPLINE.ZIP file. This file must be unzipped using PKUNZIP.EXE. A copy of PKUNZIP is included on the standard NR&D software disk and is also available at www.niobrara.com. The latest version of the DUPLINE.ZIP file is located at

ftp.niobrara.com/ucm/dupline/dupline.zip

The latest version of this document in pdf format is located at:

ftp.niobrara.com/ucm/dupline/dupline.pdf

Serial Connections to the UCM4-S

Port 1 to OLI V24 115 Fiber Optic RS-232 Converter

Port 1 of the UCM4-S is RS-232 and the OLI box is also RS-232. The OLI includes a 25-pin RS-232 connection.

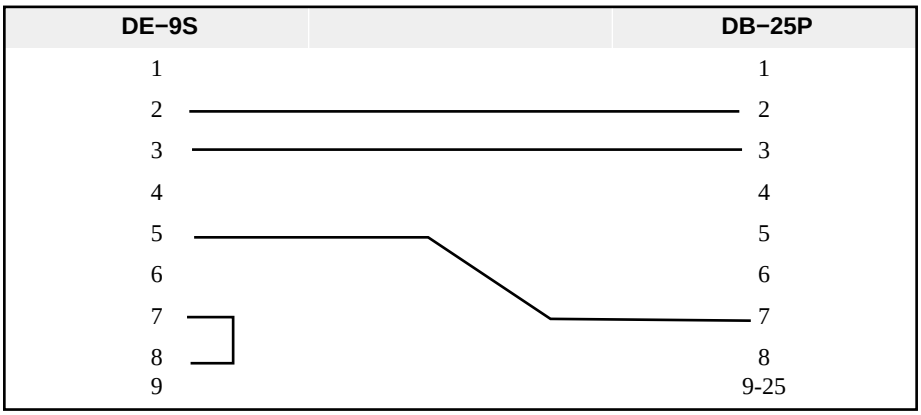

Figure 2-1 OLI RS-232 Cable Pinout

The UCM4-S Port 1 and the Optolinks must be configured for the same baud rate. The UCM application is set to 9600 baud but may be changed another setting to match the Optolink.

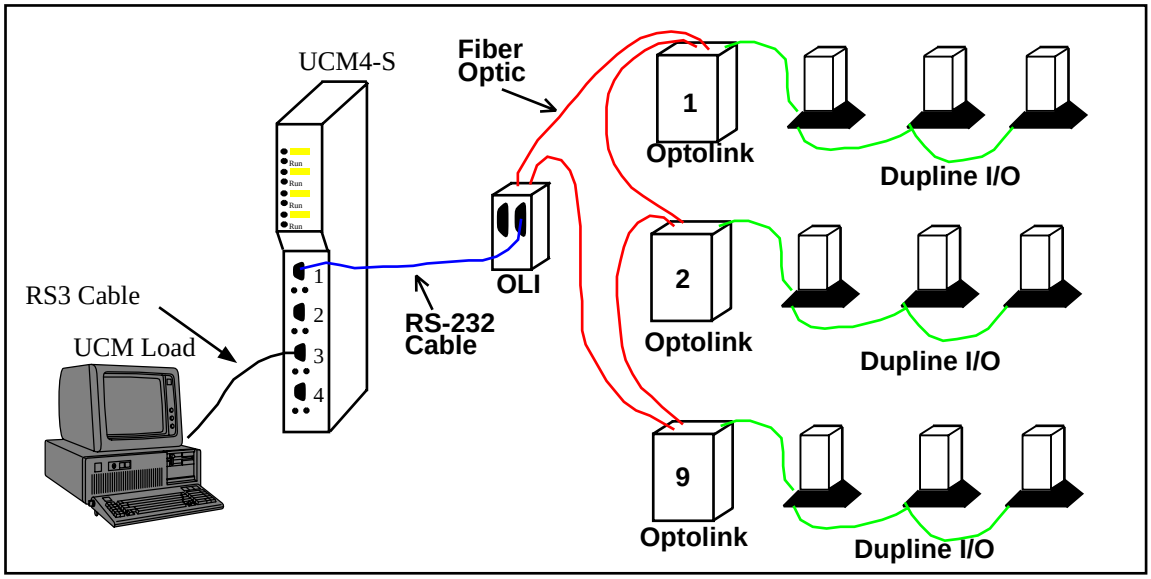

Figure 2-2 UCM4-S Layout

The system layout will be as shown in Figure 2-2. The UCM4-S Port 1 is connected to the OLI box with the RS-232 cable in Figure 2-1. The OLI box is connected to the nine Optolinks addressed 1 through 9 respectively. Each Optolink will have its own Dupline network with a 128 Channel Generator and Receivers and Transmitters.

Port 2, 3, or 4 to the Personal Computer

A physical connection must be made from the personal computer to the UCM in order to download the applications. This link may be a serial connection from a COM port on the personal computer to the RS-232 port on the UCM4-S. The Niobrara RS3 cable may be used for this connection. This cable pinout is shown in Figure 2-3.

If remote configuration is desirable, Port 2 of the UCM may be connected to a spare SY/MAX mode port of the EPE5-TCP, MEB-TCP, SPE4, or Square D NIM by means of an SC902 cable with its external power supply. The network module port should

be set for SY/MAX mode, 9600 baud, EVEN parity, 8 data bits, 1 stop bit, and BCC error checking.

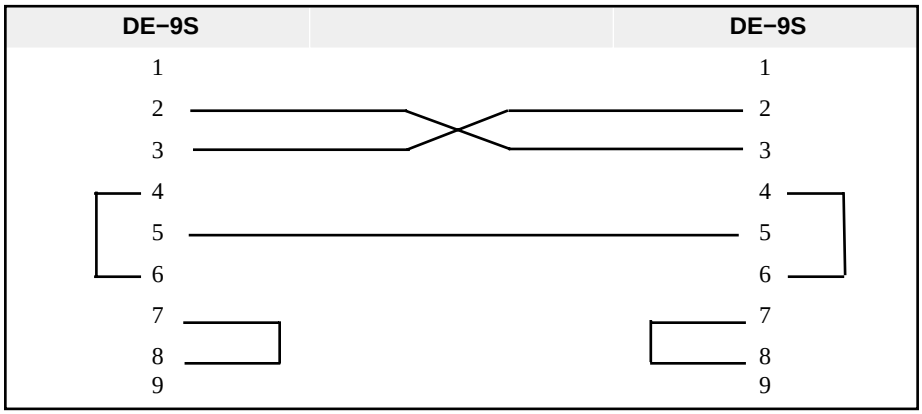

Figure 2-3 RS3 Pinout

Loading the Applications into the UCM4

Four batch files are included to assist loading the programs into the UCM4. Connect the computer to Port 2 (or Port 3 or Port 4) of the UCM4. If the computer operating system is DOS or Windows 3.x (16 bit) then run either DOS1.BAT for COM1: or DOS2.BAT for the PC's COM2:. If the computer operating system is Windows 95/98 or NT then run WIN1.BAT for COM1: or WIN2.BAT for COM2: These files will automatically load the program into the proper port and set it for Auto-Start. After completion of the loading, the green RUN light at the top of the UCM should light on Port 1.

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Register List

The UCM4 should be rack addressed for 209 registers to allow the PLC access to all data and statistics. These registers are described in the following tables:

Table 3-1 Global Control and Statistics

UCM Register	PLC I/O Direction	Description
1	Input	UCM Control - Bit 1 on to run Port1.ucm
2	Input	UCM Status - Bit 16 on if Port1 running
3	Input	UCM Line Number - normally zero
4	Input	Good Data Reply Counter
5	Input	Timeout getting echo from network count
6	Input	Timeout getting reply from network count
7	Input	Bad Checksum counter
8	Input	Optolink Fault counter
9-1	Input	Toggles with each Address Change
9-2	Input	On if timeout on echo from network
9-15	Input	On if Bad optolink checksum fault
9-16	Input	On if optolink Dupline network fault
10-1	Input	On if data from Optolink Network 1 is good
10-2	Input	On if data from Optolink Network 2 is good
10-3	Input	On if data from Optolink Network 3 is good
10-4	Input	On if data from Optolink Network 4 is good
10-5	Input	On if data from Optolink Network 5 is good
10-6	Input	On if data from Optolink Network 6 is good
10-7	Input	On if data from Optolink Network 7 is good
10-8	Input	On if data from Optolink Network 8 is good
10-9	Input	On if data from Optolink Network 9 is good

Table 3-2 Optolink No. 1

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
11	Input	A	Analog Transmitter	F2FLOW
12	Input	B	Analog Transmitter	F1FLOW
13	Input	C	Analog Transmitter	F3FLOW
14	Input	D	Analog Transmitter	PPHG
15	Input	E	Analog Transmitter	PTURG
16-1	Input	F-1	Discrete Transmitter Bit 1	PPHALAG
16-2	Input	F-2	Discrete Transmitter Bit 2	PPHALBG
16-3	Input	F-3	Discrete Transmitter Bit 3	PTURALAG
16-4	Input	F-4	Discrete Transmitter Bit 4	PTURALBG
16-5	Input	F-5	Discrete Transmitter Bit 5	DPHALAA
16-6	Input	F-6	Discrete Transmitter Bit 6	DPHALBA
16-7	Input	F-7	Discrete Transmitter Bit 7	DTURALAA
16-8	Input	F-8	Discrete Transmitter Bit 8	DTURALBA
17	Input	G	Analog Transmitter	F4FLOW
18	Input	H	Analog Transmitter	F5FLOW
19	Input	I	Analog Transmitter	DPHA
20	Input	J	Analog Transmitter	DGCLRES
21-1	Input	K	Discrete Transmitter Bit 1	DINTAL
21-2	Input	K	Discrete Transmitter Bit 2	DFIREAL
21-3	Input	K	Discrete Transmitter Bit 3	DPOWFAIL
21-4	Input	K	Discrete Transmitter Bit 4	(spare)
21-5	Input	K	Discrete Transmitter Bit 5	WATERPMP
21-6	Input	K	Discrete Transmitter Bit 6	CL2CHAN1
21-7	Input	K	Discrete Transmitter Bit 7	CL2CHAN2
21-8	Input	K	Discrete Transmitter Bit 8	(spare)
22	Input	L	Analog Transmitter	GORBALKW
23	Input	M	Analog Transmitter	NHTLEV1A
24	Input	N	Analog Transmitter	NHTLEV1B
25	Input	O	Analog Transmitter	NTHLEV2A
26	Input	P	Analog Transmitter	NTHLEV2B

Table 3-3 Optolink No. 2

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
27-1	Input	A-1	Discrete Transmitter Bit 1	EV3OPEN
27-2	Input	A-2	Discrete Transmitter Bit 2	EV3CLOSE
27-3	Input	A-3	Discrete Transmitter Bit 3	EV3FAULT
27-4	Input	A-4	Discrete Transmitter Bit 4	EV3LOCAL
27-5	Input	A-5	Discrete Transmitter Bit 5	EV4OPEN
27-6	Input	A-6	Discrete Transmitter Bit 6	EV4CLOSE
27-7	Input	A-7	Discrete Transmitter Bit 7	EV4FAULT
27-8	Input	A-8	Discrete Transmitter Bit 8	EV4LOCAL
28-1	Input	B-1	Discrete Transmitter Bit 1	EV5OPEN
28-2	Input	B-2	Discrete Transmitter Bit 2	EV5CLOSE
28-3	Input	B-3	Discrete Transmitter Bit 3	EV5FAULT
28-4	Input	B-4	Discrete Transmitter Bit 4	EV5LOCAL
28-5	Input	B-5	Discrete Transmitter Bit 5	EV6OPEN
28-6	Input	B-6	Discrete Transmitter Bit 6	EV6CLOSE
28-7	Input	B-7	Discrete Transmitter Bit 7	EV6FAULT
28-8	Input	B-8	Discrete Transmitter Bit 8	EV6LOCAL
29-1	Input	C-1	Discrete Transmitter Bit 1	EV7OPEN
29-2	Input	C-2	Discrete Transmitter Bit 2	EV7CLOSE
29-3	Input	C-3	Discrete Transmitter Bit 3	EV7FAULT
29-4	Input	C-4	Discrete Transmitter Bit 4	EV7LOCAL
29-5	Input	C-5	Discrete Transmitter Bit 5	EV8OPEN
29-6	Input	C-6	Discrete Transmitter Bit 6	EV8CLOSE
29-7	Input	C-7	Discrete Transmitter Bit 7	EV8FAULT
29-8	Input	C-8	Discrete Transmitter Bit 8	EV8LOCAL
30-1	Input	D-1	Discrete Transmitter Bit 1	EV9OPEN
30-2	Input	D-2	Discrete Transmitter Bit 2	EV9CLOSE
30-3	Input	D-3	Discrete Transmitter Bit 3	EV9FAULT
30-4	Input	D-4	Discrete Transmitter Bit 4	EV9LOCAL
30-5	Input	D-5	Discrete Transmitter Bit 5	(spare)
30-6	Input	D-6	Discrete Transmitter Bit 6	(spare)
30-7	Input	D-7	Discrete Transmitter Bit 7	(spare)
30-8	Input	D-8	Discrete Transmitter Bit 8	(spare)
31-1	Output	E-1	Discrete Receiver Bit 1	OPENEV5
31-2	Output	E-2	Discrete Receiver Bit 2	CLOSEEV5
31-3	Output	E-3	Discrete Receiver Bit 3	OPENEV6
31-4	Output	E-4	Discrete Receiver Bit 4	CLOSEEV6
31-5	Output	E-5	Discrete Receiver Bit 5	OPENEV7
31-6	Output	E-6	Discrete Receiver Bit 6	CLOSEEV7
31-7	Output	E-7	Discrete Receiver Bit 7	OPENEV8
31-8	Output	E-8	Discrete Receiver Bit 8	CLOSEEV8

Table 3-4 Optolink No. 2 (cont.)

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
32-1	Output	F-1	Discrete Receiver Bit 1	OPENEV9
32-2	Output	F-2	Discrete Receiver Bit 2	CLOSEEV9
32-3	Output	F-3	Discrete Receiver Bit 3	OPENEV3
32-4	Output	F-4	Discrete Receiver Bit 4	CLOSEEV3
32-5	Output	F-5	Discrete Receiver Bit 5	OPENEV4
32-6	Output	F-6	Discrete Receiver Bit 6	CLOSEEV4
32-7	Output	F-7	Discrete Receiver Bit 7	(spare)
32-8	Output	F-8	Discrete Receiver Bit 8	(spare)
33	Input	G	Analog Transmitter	EV3PLACE
34	Input	H	Analog Transmitter	EV4PLACE
35	Input	I	Analog Transmitter	EV5PLACE
36	Input	J	Analog Transmitter	EV6PLACE
37	Input	K	Analog Transmitter	F6FLOW
38	Input	L	Analog Transmitter	EV7PLACE
39	Input	M	Analog Transmitter	EV8PLACE
40	Input	N	Analog Transmitter	EV9PLACE
41	Input	O	Analog Transmitter	OHTLEVA
42	Input	P	Analog Transmitter	OHTLEVB

Table 3-5 Optolink No. 3

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
43-1	Input	A-1	Discrete Transmitter Bit 1	EV10OPEN
43-2	Input	A-2	Discrete Transmitter Bit 2	EV10CLOS
43-3	Input	A-3	Discrete Transmitter Bit 3	EV10FAUL
43-4	Input	A-4	Discrete Transmitter Bit 4	EV10LOCA
43-5	Input	A-5	Discrete Transmitter Bit 5	EV11OPEN
43-6	Input	A-6	Discrete Transmitter Bit 6	EV11CLOS
43-7	Input	A-7	Discrete Transmitter Bit 7	EV11FAUL
43-8	Input	A-8	Discrete Transmitter Bit 8	EV11LOCA
44-1	Input	B-1	Discrete Transmitter Bit 1	EV12OPEN
44-2	Input	B-2	Discrete Transmitter Bit 2	EV12CLOS
44-3	Input	B-3	Discrete Transmitter Bit 3	EV12FAUL
44-4	Input	B-4	Discrete Transmitter Bit 4	EV12LOCA
44-5	Input	B-5	Discrete Transmitter Bit 5	EV13OPEN
44-6	Input	B-6	Discrete Transmitter Bit 6	EV13CLOS
44-7	Input	B-7	Discrete Transmitter Bit 7	EV13FAUL
44-8	Input	B-8	Discrete Transmitter Bit 8	EV13LOCA

Table 3-6 Optolink No. 3 (cont.)

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
45-1	Output	C-1	Discrete Receiver Bit 1	(spare)
45-2	Output	C-2	Discrete Receiver Bit 2	(spare)
45-3	Output	C-3	Discrete Receiver Bit 3	(spare)
45-4	Output	C-4	Discrete Receiver Bit 4	(spare)
45-5	Output	C-5	Discrete Receiver Bit 5	OPENEV10
45-6	Output	C-6	Discrete Receiver Bit 6	CLOSEEV10
45-7	Output	C-7	Discrete Receiver Bit 7	OPENEV11
45-8	Output	C-8	Discrete Receiver Bit 8	CLOSEEV11
46-1	Output	D-1	Discrete Receiver Bit 1	OPENEV12
46-2	Output	D-2	Discrete Receiver Bit 2	CLOSEEV12
46-3	Output	D-3	Discrete Receiver Bit 3	OPENEV13
46-4	Output	D-4	Discrete Receiver Bit 4	CLOSEEV13
46-5	Output	D-5	Discrete Receiver Bit 5	OPENEV14
46-6	Output	D-6	Discrete Receiver Bit 6	CLOSEEV14
46-7	Output	D-7	Discrete Receiver Bit 7	(spare)
46-8	Output	D-8	Discrete Receiver Bit 8	(spare)
47	Input	E	Analog Transmitter	EV10PLAC
48	Input	F	Analog Transmitter	EV11PLAC
49	Input	G	Analog Transmitter	EV12PLAC
50	Input	H	Analog Transmitter	EV13PLAC
51	Input	I	Analog Transmitter	EV14PLAC
52	Input	J	Analog Transmitter	F7FLOW
53	Input	K	Analog Transmitter	F8FLOW
54	Input	L	Analog Transmitter	GPHH
55	Input	M	Analog Transmitter	GTURH
56-1	Input	N-1	Discrete Transmitter Bit 1	CLOSEEV9
56-2	Input	N-2	Discrete Transmitter Bit 2	OPENEV3
56-3	Input	N-3	Discrete Transmitter Bit 3	GTURALAH
56-4	Input	N-4	Discrete Transmitter Bit 4	GTURALBH
56-5	Input	N-5	Discrete Transmitter Bit 5	EV14OPEN
56-6	Input	N-6	Discrete Transmitter Bit 6	EV14CLOS
56-7	Input	N-7	Discrete Transmitter Bit 7	EV14FAUL
56-8	Input	N-8	Discrete Transmitter Bit 8	EV14LOCA
57	Input	O	Analog Transmitter	OBCLRES
58	Input	P	Analog Transmitter	(spare)

Table 3-7 Optolink No. 4

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
59-1	Input	A-1	Discrete Transmitter Bit 1	V575MIA1
59-2	Input	A-2	Discrete Transmitter Bit 2	V575HIA1
59-3	Input	A-3	Discrete Transmitter Bit 3	V575LOA1
59-4	Input	A-4	Discrete Transmitter Bit 4	V575MAA1
59-5	Input	A-5	Discrete Transmitter Bit 5	V575MIA2
59-6	Input	A-6	Discrete Transmitter Bit 6	V575HIA2
59-7	Input	A-7	Discrete Transmitter Bit 7	V575LOA2
59-8	Input	A-8	Discrete Transmitter Bit 8	V575MAA2
60-1	Input	B-1	Discrete Transmitter Bit 1	V595A1
60-2	Input	B-2	Discrete Transmitter Bit 2	V595B1
60-3	Input	B-3	Discrete Transmitter Bit 3	V595C1
60-4	Input	B-4	Discrete Transmitter Bit 4	V595D1
60-5	Input	B-5	Discrete Transmitter Bit 5	V595E1
60-6	Input	B-6	Discrete Transmitter Bit 6	V595F1
60-7	Input	B-7	Discrete Transmitter Bit 7	V595G1
60-8	Input	B-8	Discrete Transmitter Bit 8	V595H1 (spare)
61-1	Input	C-1	Discrete Transmitter Bit 1	V595A2
61-2	Input	C-2	Discrete Transmitter Bit 2	V595B2
61-3	Input	C-3	Discrete Transmitter Bit 3	V595C2
61-4	Input	C-4	Discrete Transmitter Bit 4	V595D2
61-5	Input	C-5	Discrete Transmitter Bit 5	V595E2
61-6	Input	C-6	Discrete Transmitter Bit 6	V595F2
61-7	Input	C-7	Discrete Transmitter Bit 7	V595G2
61-8	Input	C-8	Discrete Transmitter Bit 8	V595H2 (spare)
62-1	Input	D-1	Discrete Transmitter Bit 1	TE1HIAL
62-2	Input	D-2	Discrete Transmitter Bit 2	TE1LOAL
62-3	Input	D-3	Discrete Transmitter Bit 3	TE1SENFA
62-4	Input	D-4	Discrete Transmitter Bit 4	TE2HIAL
62-5	Input	D-5	Discrete Transmitter Bit 5	TE2LOAL
62-6	Input	D-6	Discrete Transmitter Bit 6	TE2SENFA
62-7	Input	D-7	Discrete Transmitter Bit 7	BP1RUST
62-8	Input	D-8	Discrete Transmitter Bit 8	BP1TR
63-1	Input	E-1	Discrete Transmitter Bit 1	BP2RUST
63-2	Input	E-2	Discrete Transmitter Bit 2	BP2TR
63-3	Input	E-3	Discrete Transmitter Bit 3	SPA1RUST
63-4	Input	E-4	Discrete Transmitter Bit 4	SPA1TR
63-5	Input	E-5	Discrete Transmitter Bit 5	SPA2RUST
63-6	Input	E-6	Discrete Transmitter Bit 6	SPA2TR
63-7	Input	E-7	Discrete Transmitter Bit 7	SPB1RUST
63-8	Input	E-8	Discrete Transmitter Bit 8	SPB1TR

Table 3-8 Optolink No. 4 (cont.)

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
64-1	Input	F-1	Discrete Transmitter Bit 1	SPB2RUST
64-2	Input	F-2	Discrete Transmitter Bit 2	SPB2TR
64-3	Input	F-3	Discrete Transmitter Bit 3	SPC1RUST
64-4	Input	F-4	Discrete Transmitter Bit 4	SPC1TR
64-5	Input	F-5	Discrete Transmitter Bit 5	SPC2RUST
64-6	Input	F-6	Discrete Transmitter Bit 6	SPC2TR
64-7	Input	F-7	Discrete Transmitter Bit 7	(spare)
64-8	Input	F-8	Discrete Transmitter Bit 8	(spare)
65	Input	G	Analog Transmitter	NHTCLRES
66	Input	H	Analog Transmitter	OHTCLRES
67	Input	I	Analog Transmitter	MILCLRES
68	Input	J	Analog Transmitter	DTURA
69	Input	K	Analog Transmitter	(spare)
70	Input	L	Analog Transmitter	(spare)
71	Input	M	Analog Transmitter	(spare)
72	Input	N	Analog Transmitter	(spare)
73	Input	O	Analog Transmitter	(spare)
74	Input	P	Analog Transmitter	(spare)

Table 3-9 Optolink No. 5

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
75-1	Input	A-1	Discrete Transmitter Bit 1	TPSPOWF
75-2	Input	A-2	Discrete Transmitter Bit 2	TPSINTAL
75-3	Input	A-3	Discrete Transmitter Bit 3	TPSFIAL
75-4	Input	A-4	Discrete Transmitter Bit 4	TPSFLAL
75-5	Input	A-5	Discrete Transmitter Bit 5	TP1RUST
75-6	Input	A-6	Discrete Transmitter Bit 6	TP1TR
75-7	Input	A-7	Discrete Transmitter Bit 7	TP2RUST
75-8	Input	A-8	Discrete Transmitter Bit 8	TP2TR
76-1	Input	B-1	Discrete Transmitter Bit 1	TP3RUST
76-2	Input	B-2	Discrete Transmitter Bit 2	TP3TR
76-3	Input	B-3	Discrete Transmitter Bit 3	TPV1OP
76-4	Input	B-4	Discrete Transmitter Bit 4	TPV1CL
76-5	Input	B-5	Discrete Transmitter Bit 5	TPV1FA
76-6	Input	B-6	Discrete Transmitter Bit 6	TPV2OP
76-7	Input	B-7	Discrete Transmitter Bit 7	TPV2CL
76-8	Input	B-8	Discrete Transmitter Bit 8	TP2FA
77-1	Input	C-1	Discrete Transmitter Bit 1	TPV3OP
77-2	Input	C-2	Discrete Transmitter Bit 2	TPV3CL
77-3	Input	C-3	Discrete Transmitter Bit 3	TPV3FA
77-4	Input	C-4	Discrete Transmitter Bit 4	LOWSUCT
77-5	Input	C-5	Discrete Transmitter Bit 5	LOWDELIV
77-6	Input	C-6	Discrete Transmitter Bit 6	HIGHDELV
77-7	Input	C-7	Discrete Transmitter Bit 7	(spare)
77-8	Input	C-8	Discrete Transmitter Bit 8	(spare)
78	Input	D	Analog Transmitter	TP1A
79	Input	E	Analog Transmitter	TP2A
80	Input	F	Analog Transmitter	TP3A
81	Input	G	Analog Transmitter	TPSOUFLO
82	Input	H	Analog Transmitter	EV3POSN
83	Input	I	Analog Transmitter	EV4POSN
84	Input	J	Analog Transmitter	(spare)
85	Input	K	Analog Transmitter	EV5POSN
86	Input	L	Analog Transmitter	EV6POSN
87	Input	M	Analog Transmitter	EV7POSN
88	Output	N	Analog Receiver	NHTCLSET
89	Output	O	Analog Receiver	OHTCLSET
90	Input	P	Analog Transmitter	(spare)

Table 3-10 Optolink No. 6

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
91	Input	A	Analog Transmitter	TURH_OUT
92	Input	B	Analog Transmitter	EV8POSN
93	Input	C	Analog Transmitter	EV9POSN
94	Input	D	Analog Transmitter	EV10POSN
95	Input	E	Analog Transmitter	EV11POSN
96	Input	F	Analog Transmitter	EV12POSN
97	Input	G	Analog Transmitter	EV13POSN
98	Input	H	Analog Transmitter	EV14POSN
99	Input	I	Analog Transmitter	(spare)
100-1	Input	J-1	Discrete Transmitter Bit 1	(spare)
100-2	Input	J-2	Discrete Transmitter Bit 2	(spare)
100-3	Input	J-3	Discrete Transmitter Bit 3	(spare)
100-4	Input	J-4	Discrete Transmitter Bit 4	(spare)
100-5	Input	J-5	Discrete Transmitter Bit 5	(spare)
100-6	Input	J-6	Discrete Transmitter Bit 6	(spare)
100-7	Input	J-7	Discrete Transmitter Bit 7	(spare)
100-8	Input	J-8	Discrete Transmitter Bit 8	(spare)
101	Input	K	Analog Transmitter	(spare)
102	Input	L	Analog Transmitter	(spare)
103	Input	M	Analog Transmitter	(spare)
104	Input	N	Analog Transmitter	(spare)
105	Input	O	Analog Transmitter	(spare)
106	Input	P	Analog Transmitter	(spare)

Table 3-11 Optolink No. 7

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
107	Input	A	Analog Transmitter	NHTCLSET
108	Input	B	Analog Transmitter	OHTCLSET
109	Input	C	Analog Transmitter	NHTRESID
110	Input	D	Analog Transmitter	OHTRESID
111	Input	E	Analog Transmitter	(spare)
112	Input	F	Analog Transmitter	(spare)
113	Input	G	Analog Transmitter	(spare)
114	Input	H	Analog Transmitter	(spare)
115	Input	I	Analog Transmitter	(spare)
116-1	Input	J-1	Discrete Transmitter Bit 1	(unknown)
116-2	Input	J-2	Discrete Transmitter Bit 2	(unknown)
116-3	Input	J-3	Discrete Transmitter Bit 3	(unknown)
116-4	Input	J-4	Discrete Transmitter Bit 4	(unknown)
116-5	Input	J-5	Discrete Transmitter Bit 5	(unknown)
116-6	Input	J-6	Discrete Transmitter Bit 6	(unknown)
116-7	Input	J-7	Discrete Transmitter Bit 7	(unknown)
116-8	Input	J-8	Discrete Transmitter Bit 8	(unknown)
117	Input	K	Analog Transmitter	(spare)
118	Input	L	Analog Transmitter	(spare)
119	Input	M	Analog Transmitter	(spare)
120	Input	N	Analog Transmitter	(spare)
121	Input	O	Analog Transmitter	(spare)
122	Input	P	Analog Transmitter	(spare)

Table 3-12 Optolink No. 8

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
123	Input	A	Analog Transmitter	F6_OUT
124	Input	B	Analog Transmitter	F7_OUT
125	Input	C	Analog Transmitter	F8_OUT
126	Input	D	Analog Transmitter	F9_OUT
127	Input	E	Analog Transmitter	MILPHOUT
128	Input	F	Analog Transmitter	PHGOUT
129	Input	G	Analog Transmitter	PHHOUT
130	Input	H	Analog Transmitter	MILTOUT
131	Input	I	Analog Transmitter	TURG_OUT
132-1	Input	J-1	Discrete Transmitter Bit 1	(unknown)
132-2	Input	J-2	Discrete Transmitter Bit 2	(unknown)
132-3	Input	J-3	Discrete Transmitter Bit 3	(unknown)
132-4	Input	J-4	Discrete Transmitter Bit 4	(unknown)
132-5	Input	J-5	Discrete Transmitter Bit 5	(unknown)
132-6	Input	J-6	Discrete Transmitter Bit 6	(unknown)
132-7	Input	J-7	Discrete Transmitter Bit 7	(unknown)
132-8	Input	J-8	Discrete Transmitter Bit 8	(unknown)
133	Input	K	Analog Transmitter	(spare)
134	Input	L	Analog Transmitter	(spare)
135	Input	M	Analog Transmitter	(spare)
136	Input	N	Analog Transmitter	(spare)
137	Input	O	Analog Transmitter	(spare)
138	Input	P	Analog Transmitter	(spare)

Table 3-13 Optolink No. 9

UCM Register	PLC I/O Direction	Dupline Address	Description	Genesis Tag
139	Input	A	Analog Transmitter	NHTE
140	Input	B	Analog Transmitter	F1_OUT
141	Input	C	Analog Transmitter	NHTW
142-1	Input	D-1	Discrete Transmitter Bit 1	D1
142-2	Input	D-2	Discrete Transmitter Bit 2	A4
142-3	Input	D-3	Discrete Transmitter Bit 3	D3
142-4	Input	D-4	Discrete Transmitter Bit 4	D4
142-5	Input	D-5	Discrete Transmitter Bit 5	A8
142-6	Input	D-6	Discrete Transmitter Bit 6	D6
142-7	Input	D-7	Discrete Transmitter Bit 7	SOUNDER
142-8	Input	D-8	Discrete Transmitter Bit 8	(spare)
143-1	Input	E-1	Discrete Transmitter Bit 1	E1
143-2	Input	E-2	Discrete Transmitter Bit 2	E2
143-3	Input	E-3	Discrete Transmitter Bit 3	E3
143-4	Input	E-4	Discrete Transmitter Bit 4	E4
143-5	Input	E-5	Discrete Transmitter Bit 5	E5
143-6	Input	E-6	Discrete Transmitter Bit 6	E6
143-7	Input	E-7	Discrete Transmitter Bit 7	E7
143-8	Input	E-8	Discrete Transmitter Bit 8	E8
144-1	Input	F-1	Discrete Transmitter Bit 1	F1
144-2	Input	F-2	Discrete Transmitter Bit 2	F2
144-3	Input	F-3	Discrete Transmitter Bit 3	F3
144-4	Input	F-4	Discrete Transmitter Bit 4	F4
144-5	Input	F-5	Discrete Transmitter Bit 5	F5
144-6	Input	F-6	Discrete Transmitter Bit 6	F6
144-7	Input	F-7	Discrete Transmitter Bit 7	F7
144-8	Input	F-8	Discrete Transmitter Bit 8	F8
145	Input	G	Analog Transmitter	F3_OUT
146	Input	H	Analog Transmitter	F2_OUT
147	Input	I	Analog Transmitter	OHTL
148	Input	J	Analog Transmitter	F4_OUT
149	Input	K	Analog Transmitter	F5_OUT
150	Input	L	Analog Transmitter	MILCLRES
151	Input	M	Analog Transmitter	DGCLRES
152	Input	N	Analog Transmitter	OBCLRES
153	Input	O	Analog Transmitter	(spare)
154	Input	P	Analog Transmitter	(spare)

Table 3-14 Optolink Statistical Counters

UCM Register	PLC I/O Direction	Description
155-160	Input	Spare
161	Input	Optolink 1 Good Reply Counter
162	Input	Optolink 2 Good Reply Counter
163	Input	Optolink 3 Good Reply Counter
164	Input	Optolink 4 Good Reply Counter
165	Input	Optolink 5 Good Reply Counter
166	Input	Optolink 6 Good Reply Counter
167	Input	Optolink 7 Good Reply Counter
168	Input	Optolink 8 Good Reply Counter
169	Input	Optolink 9 Good Reply Counter
160	Input	Spare
171	Input	Optolink 1 Timeout Counter
172	Input	Optolink 2 Timeout Counter
173	Input	Optolink 3 Timeout Counter
174	Input	Optolink 4 Timeout Counter
175	Input	Optolink 5 Timeout Counter
176	Input	Optolink 6 Timeout Counter
177	Input	Optolink 7 Timeout Counter
178	Input	Optolink 8 Timeout Counter
179	Input	Optolink 9 Timeout Counter
180	Input	Spare
181	Input	Optolink 1 Dupline Fault Counter
182	Input	Optolink 2 Dupline Fault Counter
183	Input	Optolink 3 Dupline Fault Counter
184	Input	Optolink 4 Dupline Fault Counter
185	Input	Optolink 5 Dupline Fault Counter
186	Input	Optolink 6 Dupline Fault Counter
187	Input	Optolink 7 Dupline Fault Counter
188	Input	Optolink 8 Dupline Fault Counter
189	Input	Optolink 9 Dupline Fault Counter
190	Input	Spare
191	Input	Optolink 1 Checksum Fault Counter
192	Input	Optolink 2 Checksum Fault Counter
193	Input	Optolink 3 Checksum Fault Counter
194	Input	Optolink 4 Checksum Fault Counter
195	Input	Optolink 5 Checksum Fault Counter
196	Input	Optolink 6 Checksum Fault Counter
197	Input	Optolink 7 Checksum Fault Counter
198	Input	Optolink 8 Checksum Fault Counter
199	Input	Optolink 9 Checksum Fault Counter

Table 3-15 Optolink Statistical Counters (cont.)

UCM Register	PLC I/O Direction	Description
200	Input	Spare
201	Input	Optolink 1 Bad Address Reply Counter
202	Input	Optolink 2 Bad Address Reply Counter
203	Input	Optolink 3 Bad Address Reply Counter
204	Input	Optolink 4 Bad Address Reply Counter
205	Input	Optolink 5 Bad Address Reply Counter
206	Input	Optolink 6 Bad Address Reply Counter
207	Input	Optolink 7 Bad Address Reply Counter
208	Input	Optolink 8 Bad Address Reply Counter
209	Input	Optolink 9 Bad Address Reply Counter

4

Operation

Overview

The PORT1 program runs continuously copying data from the PLC outputs to the Dupline Receivers and from the Dupline Transmitters to the PLC inputs. The nine Dupline networks are polled in order from one to nine using a single message that writes the all output data and reads the input data for Groups A-P. Observations on a single Optolink indicate a system throughput of approximately 182mS per poll and 9600 baud. With nine Optolinks the UCM should update all of the I/O once every 1.8 seconds or better.

Data Validity and Safety

Data integrity is checked by means of a checksum in the message structure. The UCM application generates the appropriate checksum on all outbound messages and verifies the checksum on all replies. If the data is considered valid by the UCM then a bit in register 10 will be set that corresponds to the polled Optolink will be set. If register 10 bit 1 is set then the data from Dupline network 1 is considered valid. A timeout of the echo of the command, a timeout of the reply from the Optolink, a bad checksum in the reply, or a Dupline Fault message will cause the appropriate bit in register 10 to be cleared and the data should not be considered valid.

There are statistical counters that may be used to monitor the activity of the system. There are general counters for the completion of a good reply, timeouts, bad checksums, as well as specific counters for each Optolink.

NOTE: The Optolink network is simply a loop where every message gets echoed around until it returns to the UCM. If a fiber link is broken or if any Optolink device is powered down then the whole communication network will fail. Echo timeout counters will increment on all devices and it will be impossible to determine from the UCM exactly which devices failed.

NOTE: In the event of an Optolink network failure, the output data on a given Dupline network may remain active even though the UCM and PLC no longer have con-

trol of the system. It appears that the local Optolink does not have the ability to timeout on a loss of network activity and it will keep its "virtual Transmitters" active until it is powered off or the Dupline network is stopped. This loss of control may have serious consequences! The system should be designed to accommodate this type of operation.

Bit 1 of Register 9 changes state with each loop through polling the Optolinks. During normal operation this bit should change state approximately every 185mS and if timeouts are occurring every 300 or 500mS. This bit may be used to reset a timer in the PLC program to function as a watchdog to ensure the accuracy of the data. If the Port 1 application should halt or if the serial cable were disconnected from the Port 1 then this bit would stop changing state and the PLC could sound an alarm to indicate trouble.

UCM Lights

The Green RUN light on the top panel of the module should be on when the port is running the application. If this light is not on the the program is either not loaded or has been stopped.

The Red User light on the top panel of the module indicates an error is occurring such as a timeout or bad checksum. Normally this light will be off. When it becomes illuminated then the user should check the statistical counters to determine the cause of the error.

The Yellow TX light directly under Port 1 indicates the flow of data from the UCM. This light should normally be blinking on and off during normal communication. If the green run light is on but this TX light never blinks then check that the serial cable is connected to Port 1 and wired properly. Be sure to check that Pins 7 and 8 are jumpered together.

The Yellow RX light directly under Port 1 indicates the flow of data from the Optolink network to the UCM. This light will blink with every character that is received by the UCM. If the TX light is blinking but the RX light is not blinking then check the Optolink Network for integrity as well as all of the Optolinks to be sure that they are powered up. Every message that the UCM generates must be echoed around the Optolink network and back to the UCM so the RX light should come one every time the TX light does. The Optolink reply comes immediately after the command so the UCM RX light should blink a little longer than the TX light since the command echo + reply is longer than the just the command.

PLC Inputs and Outputs

The UCM's rack addressable registers will always have a Status (SY/MAX bits 17 through 32) of either xA000 (PLC writeable Output) or xE000 (PLC read-only Input). By default the UCM's registers default to PLC Outputs and have a Status of xA000. If a register is modified by the UCM application or by an external SY/MAX write through one of the serial ports then that register changes from a PLC output (xA000) to a PLC input (xE000).

Most of the registers in this application are PLC Inputs and have a status of xE000. The registers that map to Dupline Receivers are PLC Outputs and have a status of xA000. Do not write to these registers from one of the serial ports on the UCM or the

output will change to an input and the PLC will no longer be able to modify the value. If this happens then the UCM will need to have its power cycled to return to the normal I/O mapping.